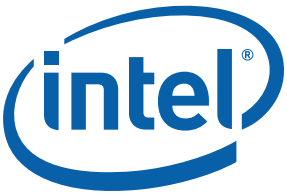

Intel® I/O Controller Hub 10 (ICH10) Family

Specification Update

June 2008

Notice: The Intel® I/O Controller Hub 10 (ICH10) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 319974-001

This document contains information on products in the design phase of development.

All products, platforms, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice. All dates specified are target dates, are provided for planning purposes only and are subject to change.

This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local sales office that you have the latest datasheet before finalizing a design.

The Intel® I/O Controller Hub 10 (ICH10) Family chipset component may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

I^2C is a two-wire communications bus/protocol developed by Philips. SMBus is a subset of the I^2C bus/protocol and was developed by Intel. Implementations of the I^2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel® Active Management Technology requires the computer system to have an Intel® AMT-enabled chipset, network hardware and software, as well as connection with a power source and a corporate network connection. Setup requires configuration by the purchaser and may require scripting with the management console or further integration into existing security frameworks to enable certain functionality. It may also require modifications of implementation of new business processes. With regard to notebooks, Intel AMT may not be available or certain capabilities may be limited over a host OS-based VPN or when connecting wirelessly, on battery power, sleeping, hibernating or powered off. For more information, see www.intel.com/technology/platform-technology/intel-amt/

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain computer system software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

No computer system can provide absolute security under all conditions. Intel® Trusted Execution Technology (Intel® TXT) requires a computer system with Intel Virtualization Technology, an Intel TXT-enabled processor, chipset, BIOS, Authenticated Code Modules and an Intel TXT-compatible measured launched environment (MLE). The MLE could consist of a virtual machine monitor, an OS or an application. In addition, Intel TXT requires the system to contain a TPM v1.2, as defined by the Trusted Computing Group and specific software for some uses. For more information, see http://www.intel.com/technology/security

Home networking capability and many Intel® Viiv™ technology-based usage models will require additional hardware devices, software or services. Functionality of Intel® Viiv™ technology verified devices will vary; check product details for desired features. System and component performance and functionality will vary depending on your specific hardware and software configurations. See www.intel.com/go/viiv_info for more information.

Intel® High Definition Audio requires a system with an appropriate Intel chipset and a motherboard with an appropriate codec and the necessary drivers installed. System sound quality will vary depending on actual implementation, controller, codec, drivers and speakers. For more information about Intel® HD audio, refer to http://www.intel.com/

Contents

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Revision History

Revision	Description	Date
-001	• Initial Release.	June 2008

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel ® I/O Controller Hub 10 (ICH10) Family Datasheet	319973-001

Nomenclature

Errata are design defects or errors. Errata may cause the ICH10's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the ICH10 product family. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping	Status	ERRATA
	A0 Consumer		
1	X	No Fix	Intel ICH10 Consumer UHCI Hang with USB Reset
2	X	No Fix	Intel ICH10 Consumer THRM Polarity on SMBus
3	X	No Fix	Intel ICH10 Consumer High Speed (HS) USB 2.0 D+ and D- Maximum Driven Signal Level
4	X	No Fix	Intel ICH10 Consumer PET Alerts on SMBus
5	X	No Fix	Intel ICH10 Consumer SMBus Host Controller May Hang
6	X	No Fix	Intel ICH10 LAN_PHY_PWR_CTRL Functionality

Specification Changes

Spec Change Number	Stepping	SPECIFICATION CHANGES
	A0 Consumer	
		There are no Specification Changes in the revision of the Specification Update

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
		There are no Specification Clarifications in the revision of the Specification Update

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
		There are no Documentation Changes in the revision of the Specification Update

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Identification Information

Markings

ICH10 Consumer Stepping	S-Spec	Top Marking	Notes
A0	SLB8R	AF82801JIB	82801JIB ICH10 (Base)
A0	SLB8S	AF82801JIR	82801JIR ICH10R

Intel® ICH10 Device and Revision Identification

Table: 2-27 ICH10 Consumer Device and Revision ID Table

Device Function	Description	Intel® ICH10 Dev ID	ICH10 A0 Rev ID	Comments
D31:F0	LPC	3A16h	00h	ICH10R
		3A18h	00h	ICH10 (Consumer Base)
D31:F21	SATA	3A20h	00h	Non-AHCI and Non-RAID Mode (Ports 0,1, 2 and 3)
		3A22h	00h	AHCI Mode (Ports 0-5)
		3A25h3	00h	RAID 0/1/5/10 mode
D31:F51	SATA	3A26h	00h	Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3A30h	00h	
D31:F6	Thermal	3A32h	00h	
D30:F0	DMI to PCI Bridge	244Eh	A0h	
D29:F0	USB UHCI #1	3A34h	00h	
D29:F1	USB UHCI #2	3A35h	00h	
D29:F2	USB UHCI #3	3A36h	00h	
D29:F3	USB UHCI #6	3A39h	00h	Note: Device and Revision ID is always the same as D26:F2.
D29:F7	USB EHCI #1	3A3Ah	00h	
D26:F0	USB UHCI #4	3A37h	00h	
D26:F1	USB UHCI #5	3A38h	00h	
D26:F2	USB UHCI #6	3A39h	00h	
D26:F7	USB EHCI #2	3A3Ch	00h	
D27:F0	Intel® High Definition Audio	3A3Eh	00h	
D28:F0	PCI Express* Port 1	3A40h	00h	
D28:F1	PCI Express Port 2	3A42h	00h	
D28:F2	PCI Express Port 3	3A44h	00h	
D28:F3	PCI Express Port 4	3A46h	00h	

Table: 2-27 ICH10 Consumer Device and Revision ID Table

Device Function	Description	Intel® ICH10 Dev ID	ICH10 A0 Rev ID	Comments
D28:F4	PCI Express Port 5	3A48h	00h	
D28:F5	PCI Express Port 6	3A4Ah	00h	
D25:F0	LAN	3A4Ch2	00h	

NOTES:

1. ICH10 contains two SATA devices. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3A4Ch is used. Refer to the 82567 GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.
3. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.

Errata

1. Intel ICH10 Consumer UHCI Hang with USB Reset

Problem: When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang.

Note: The issue has only been replicated in a synthetic reset test environment.

Implication: System may hang.

Workaround: BIOS workaround available. Contact your Intel field representative for the latest BIOS information.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

2. Intel ICH10 Consumer THRM Polarity on SMBus

Problem: When THRM#_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

Implication: If the THRM#_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#_POL is set to low, value is correct.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

3. Intel ICH10 Consumer High Speed (HS) USB 2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH10 Consumer may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix.

4. Intel ICH10 Consumer PET Alerts on SMBus

Problem: When using the ICH Consumer SMBus for Platform Event Trap (PET) alerts on a system with the Intel® Management Engine (ME) enabled, the SMBus packet headers may be corrupted if all of the following conditions are met:

- SMBus slave is the target of an external PET generating master on SMBus/SMLink
- The ME is in the middle of M0-M1 transitions
- SMBus slave receives back-to-back PET alerts of which some PET alerts are incomplete (i.e. the packet is truncated to less than 6 bytes)

Note: This issue has only been observed under a synthetic test environment.

Implication: ME firmware may stop functioning, which could cause a system hang.

Workaround: None

Status: No Fix.

5. Intel ICH10 Consumer SMBus Host Controller May Hang

Problem: During heavy SMBus traffic utilization, the ICH10 Consumer SMBus host controller may attempt to start a transaction while the bus is busy.

Note: This issue has only been observed under a synthetic test environment.

Implication: May cause the SMBus host controller to hang.

- After boot:
  - — SMBus host controller transaction may not complete.
  - — External master transaction in progress targeting ICH10 Consumer SMBus slave may get NACK or timeout.
  - — There is no impact to any other transaction that was in progress by an external master.
- This issue has not been observed during boot as SMBus utilization tends to be light.

Workaround: BIOS workaround available. Contact your Intel field representative for the latest BIOS information.

Status: No Fix.

6. Intel ICH10 LAN_PHY_PWR_CTRL Functionality

Problem: LAN_PHY_PWR_CTRL output is driven low by the ICH10 during a host reset with or without power cycle for up to 3 RTC clock cycles due to the pin momentarily being configured as an output GPIO.

- LAN_PHY_PWR_CTRL functionality requires a soft strap setting in the SPI descriptor and use of the integrated LAN controller in ICH10 with the Intel® 82567 PHY.

Implication: Functional failures such as system hangs or link loss with dropped packets have been observed when LAN_PHY_PWR_CTRL is tied to the LAN_DISABLE_N pin on the Intel 82567.

Note: There are no functional implications if the pin is configured as GPIO12.

For ICH10 Consumer based platforms:

- Intel ME-Enabled Platforms: An Intel ME FW workaround will be provided in the PC FW release.
  - — Both the Intel ME Disable bits in the SPI flash descriptor (ICHSTRP0 bit 0 & MCHSTRP0 bit 0) must be set to 0 to enable the ME FW workaround.
  - — MCHSTRP0 bit 7 in the SPI flash descriptor can be set to disable all other ME FW based features while keeping the Intel ME FW workaround enabled.
- Non Intel ME-Enabled Platforms: Remove LAN_PHY_PWR_CTRL Support on the Platform.
  - — Isolate the LAN_PHY_PWR_CTRL signal from the LAN_DISABLE_N pin.
  - — LAN_DISABLE_N has a weak integrated pull-up resistor and the Intel 82567 PHY will always remained enabled with this implementation.

Status: ICH10 Consumer: No Fix. One of the proposed workarounds must be implemented. For steppings affected, see the *Summary Table of Changes*.

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Specification Changes

There are no Specification Changes in the revision of the Specification Update.

Specification Clarifications

There are no Specification Clarifications in the revision of the Specification Update.

Document Changes

There are no Documentation Changes in the revision of the Specification Update.

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